IFW

AF

Attorney's Docket No.: 10559/188001/P8091-ADI APD2799-1-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Bradley C. Aldrich et al. Art Unit: 2613
Serial No.: 09/590,028 Examiner: Y. Young Lee
Assignee : Intel Corporation
Analog Devices, Inc.
Filed : June 7, 2000
Title : ADAPTIVE EARLY EXIT TECHNIQUES IN IMAGE CORRELATION

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF ON APPEAL

(1) Real Party in Interest

This case is assigned of record to Intel Corporation, who is hence the real party in interest.

(2) Related Appeals and Interferences

There are no known related appeals and/or interferences.

(3) Status of Claims

Claims 1-27 are pending in the application. Claims 1-16 and 23-27 have been withdrawn. Claims 17-22 are rejected and are being appealed.

(4) Status of Amendments

No amendment has been filed after final rejection.

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

October 12, 2004
Date of Deposit

R. P. Ippolito
Signature

Roxanne Ippolito
Typed or Printed Name of Person Signing Certificate

10/18/2004 YPOLITE1 00000011 09590028
01 FC:1402 340.00 OP

(5) Summary of Invention

The present application teaches systems and techniques that may be used for image compression. Some existing image compression techniques use a technique referred to as "motion estimation." In motion estimation, distortion between a source block and different search blocks is calculated to determine which of the search blocks has the lowest distortion with respect to the source block (i.e., the search block that is most like the source block). (Please see page 1, lines 6-10 of the specification).

Distortion calculation may be performed using a sum of absolute difference (SAD) calculation. (Please see page 2, lines 16-17 of the specification). The SAD calculation compares subdivisions of the source block with corresponding subdivisions of a particular search block, and sums the absolute differences determined in the comparisons. (Please see page 3, lines 4-12, and Figure 1 of the specification).

However, motion estimation techniques are generally computationally intensive. Systems and techniques according to the present application may reduce the computational load by providing for early exit strategies for image processing.

The features of independent claim 17 may be described using an example from the application, which discusses distortion calculation for a generally homogeneous image using a partial SAD calculation with n accumulators.

During an image processing operation, a first SAD calculation may be performed to determine an initial minimum distortion value between the source block and a first search block. The minimum distortion value is referred to as "Least." (Please see page 10, lines 1-3).

For subsequent calculations (e.g., for determining the distortion between the source block and a second search block), the current value of -"Least"/n is loaded into each of the n accumulators. (Please see page 9, lines 21-24). In this partial SAD example, each of the n accumulators performs 1/n of the distortion calculations for each search block comparison. In the example, SAD calculations are performed until the sign bit of at least one of the accumulators changes.

At that point, the distortion is greater than "Least"/n, and (for the example of a generally homogeneous image), the distortion between the source block and the second search block is greater than the distortion between the source block and the first search block. (Please see page 10, lines 4-6). The calculation is then exited (an "early exit," since fewer than all of the comparison calculations where performed). The distortion between the source block and a third search block is then performed.

If the sign bit of the accumulators does not change, the distortion between the source block and the second search block is less than the distortion between the source block and the first search block. (Please see page 10, lines 3-4). The value of "Least" is updated with the new minimum distortion, and the distortion between the source block and the third search block is then performed.

In the context of this example, the elements of claim 17 are the following. The "plurality of image processing elements" include the n accumulator circuits. The "circuit that stores first states of the image processing elements at a time of a specified image processing result" stores the states of the accumulators corresponding to an early exit condition (the "specified image processing result"). The "early exit circuit

that determines a completing of a calculation based on comparing current states with the first states, wherein the current states of said image processing elements are characterized by one or more characteristics of said image processing elements at a current time" is a circuit that compares the first states of the accumulators to the current states to determine whether the early exit condition has been met. For the example above, the characteristics include the value of a sign bit of an accumulator.

Claim 17 may be implemented in other ways. In other examples of partial SAD calculations, different numbers of accumulators may need to switch sign to establish an early exit. (Please see page 10, lines 9-11). Early exits may also be established for full SAD calculations (where the distortion between the source block and a particular search block is computed by a single accumulator rather than multiple accumulators each performing part of the SAD calculation).

(6) Grounds of Rejection

Claims 17-22 stand rejected under 35 U.S.C. 102(e) as allegedly being anticipated by U.S. Patent No. 6,539,541 to Geva ("Geva").

(7) Argument

I. Rejection Under 35 U.S.C. 102(e) over Geva

Claims 17-22 were rejected under 35 U.S.C. 102(e) in office actions with mailing dates of September 8, 2003 ("the first office action"), February 12, 2004 ("the second office action"), and June 18, 2004 ("the third office action").

Claim 17 and its dependent claims 18-22

Claim 17 stands rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Geva. This rejection is improper at least because Geva does not teach or suggest all elements of claim 17. The rejection of dependent claims 18-22 is improper due to their dependence on independent claim 17, and for additional reasons outlined below.

The office action incorrectly alleges that Geva teaches all elements of claim 17

Geva neither teaches nor suggests the following features of claim 17: (a) a circuit that stores first states of said image processing elements at a time of a specified image processing result; and (b) an early exit circuit that determines a completion of a calculation based on comparing current states with said first states, wherein the current states of said image processing elements are characterized by one or more characteristics of said image processing elements at a current time.

First, Geva neither teaches nor suggests "a circuit that stores first states of said image processing elements at a time of a specified image processing result," as recited in claim 17.

In the first office action, only system 100 of Figure 1 of Geva is identified as the plurality of image processing elements.

In the second office action, elements 102-138 of Geva (the constituents of system 100) are identified as "image processing elements." Elements 102-138 of Geva include: processor 102, cache memory 104, processor bus 110, graphics controller 112, bridge/memory controller 114, memory 116, first input/output bus 120, network controller 122, display device controller 124, bus bridge 126, camera 128, second I/O bus 130, data storage device

132, keyboard interface 134, user input interface 136, and audio controller 138.

Although it is noted that Figure 1 of Geva includes a camera 128, Geva does not discuss image processing at all.

Assuming (for the purposes of argument) that the above-referenced elements may be said to be a plurality of image processing elements, claim 17 further requires "a circuit that stores first states of said image processing elements at a time of a specified image processing result." There is no teaching or suggestion in Geva that such a circuit exists, or that the state of elements 102-138 be stored at all. There is certainly no teaching or suggestion of a circuit that stores first states of elements 102-138 at a time of a specified image processing result.

The first office action asserts Geva teaches this feature in figures 1, 4, and 5, and equates the "first states" of claim 17 with the counting variable "n" of FIG. 4.

It should be noted at the outset that Geva is directed to a method of constructing and unrolling speculatively counted loops (see the Abstract of Geva). Geva is thus directed to systems and techniques for compiling code, and is not directed to image processing. As Geva explains in the very first paragraph of the Detailed Description section, "Although the following embodiments are described with reference to C compilers, other embodiments are applicable to other types of programming languages that use compilers. The same techniques and teachings can easily be applied to other embodiments and other types of compiled object code." (Please see column 3, lines 60-65 of Geva).

In Geva, a loop is characterized as a "counted loop" if the number of iterations that the loop will execute is determined

once execution reaches the loop (see column 1, lines 26-28 of Geva). A "speculatively counted loop" satisfies all the requirements of a counted loop except for the characteristic that a speculatively counted loop has a loop upper bound that has not been proven to be loop invariant. See column 9, lines 53-56 of Geva. Loop unrolling is described, e.g., in column 8, lines 1-15.

Returning to the rejection, the variable "n" does not represent any state of an image processing element, let alone "first states of said image processing elements at a time of a specified image processing result." The variable "n" merely designates the number of iterations of the loop being executed. (Please see Figures 4A, 4B, and 4C of Geva, which illustrate three different versions of a loop).

The office action appears to disregard particular features of claims 17-22 including functional language, for example, that the circuit of claim 17 "stores first states of said image processing elements at a time of a specified image processing result." However, functional limitations may not be disregarded.

For example, MPEP 2173.05(g) states that "There is nothing inherently wrong with defining some part of an invention in functional terms." "A functional limitation must be evaluated and considered, just like any other limitation of the claim..." The Federal Circuit has recently affirmed that functional limitations are now entitled to patentable weight. "A patent applicant is free to recite features of an apparatus either structurally or functionally." *In re Schreiber*, 128 F.3d 1473, 1478, 44 USPQ.2d 1429, 1432 (Fed. Cir. 1997).

Since Geva neither teaches nor suggests "a circuit that stores first states of said image processing elements at a time

of a specified image processing result," claim 17 is clearly patentable over Geva.

Claim 17 is further patentable over Geva because Geva neither teaches nor suggests "an early exit circuit that determines a completion of a calculation based on comparing current states with said first states, wherein the current states of said image processing elements are characterized by one or more characteristics of said image processing elements at a current time," as recited in claim 17.

The office action alleges that FIG. 4 teaches this element, and equates current states with the indicia "i" and first states with the counting variable "n." Again, FIGS. 4A to 4C show three different versions of a loop. Geva explains that "The loop counter or control of all three versions is represented by 'i' and the termination count is represented by 'n.'" (Please see column 16, lines 41-43 of Geva).

Since Geva neither teaches nor suggests this additional feature of claim 17, claim 17 is patentable over Geva. For at least these reasons, claims 18-22, which depend from claim 17 are also patentable over Geva.

Claim 18

Claim 18 stands rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Geva. This rejection is improper at least because Geva does not teach or suggest all elements of claim 18.

Geva neither teaches nor suggests that "said characteristics include arithmetic states of said image processing elements," as recited in claim 18.

The first office action alleges that "With respect to claims 18-22, the image processing elements 100 include arithmetic states of groups 102; sign bits of accumulators

(i.e., arithmetic operations) therein; and a video camera 128." (Please see page 4 of the first office action).

In the same (first) office action, the "current states" were identified with the counting element (i) of Geva. Thus, the "characteristics" of claim 18 must be characteristics of element (i). However, according to claim 18, the "characteristics" must include arithmetic states of the image processing elements (identified as element 102 here). An arithmetic state of a counting element (i) cannot be said to be an arithmetic state of the processor 102.

Claim 19

Claim 19 stands rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Geva. This rejection is improper at least because Geva does not teach or suggest all elements of claim 19.

Geva neither teaches nor suggests that "said image processing elements include accumulators therein, and said characteristics include sign bits of said accumulators," as recited in claim 19.

Again, the first office action alleges that "With respect to claims 18-22, the image processing elements 100 include arithmetic states of groups 102; sign bits of accumulators (i.e., arithmetic operations) therein; and a video camera 128." (Please see page 4 of the first office action).

As noted above, the "characteristics" of claim 19 must be characteristics of element (i) in order to be consistent with the rejection of claim 17. However, a person of ordinary skill in the data processing arts would presume that a counting element in data processing does not have an associated sign bit, since counting uses integers beginning with the number one, and

does not use negative numbers. Further, a person of ordinary skill in the data processing arts would presume that counting would be performed with a counter, and not with an accumulator.

Claim 22

Claim 22 stands rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Geva. This rejection is improper at least because Geva does not teach or suggest all elements of claim 22.

Geva neither teaches nor suggests that "wherein said characteristics comprise states of groups of said image processing elements," as recited in claim 22.

Again, the first office action alleges that "With respect to claims 18-22, the image processing elements 100 include arithmetic states of groups 102; sign bits of accumulators (i.e., arithmetic operations) therein; and a video camera 128." (Please see page 4 of the first office action).

As noted above, the "characteristics" of claim 22 must be characteristics of element (i) in order to be consistent with the rejection of claim 17. However, the counting element (i) does not have characteristics that are states of groups of image processing elements. Additionally, the first office action does not identify any feature of Geva corresponding to "groups" of image processing elements. Instead, the first office action refers to "groups 102," which misidentifies element 102 of Geva, which is a processor.

The brief fee of $340 is enclosed. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 10/12/04

Linda G. Gunderson
Reg. No. 46,341
Attorney for Intel Corporation

Fish & Richardson P.C.
Customer Number: 20985
12390 El Camino Real
San Diego, California 92130
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

Appendix of Claims

17. An apparatus, comprising:

a plurality of image processing elements;

a circuit that stores first states of said image processing elements at a time of a specified image processing result; and

an early exit circuit that determines a completion of a calculation based on comparing current states with said first states, wherein the current states of said image processing elements are characterized by one or more characteristics of said image processing elements at a current time.

18. An apparatus as in claim 17, wherein said characteristics include arithmetic states of said image processing elements.

19. An apparatus as in claim 18, wherein said image processing elements include accumulators therein, and said characteristics include sign bits of said accumulators.

20. An apparatus as in claim 17, further comprising a video obtaining element.

21. An apparatus as in claim 20, wherein said video obtaining element is a video camera.

22. An apparatus as in claim 17, wherein said characteristics comprise states of groups of said image processing elements.